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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,314	12/21/2000	Philip W. Diodato	8-35-22	5870

7590 12/27/2001

Docket Administrator (RooM. 3C-512)
Lucent Technologies Inc.
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EXAMINER
NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/27/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,314	DIODATO ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8, drawn an integrated circuit, classified in class 257, subclass 296 and wherein:

II. Claims 9-24, drawn to a process for forming an integrated circuit, classified in class 438, subclass +1.

The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, since the product of the Group I invention could be made by another and materially different process from those of the Group II invention. For example, as an alternative in claim 9, rather than forming first wiring layer and a portion of a second wiring layer over the substrate and then opening a window through the first wiring layer and a portion of a second wiring layer, selectively depositing to form first wiring layer and a portion of a second wiring layer over the substrate and a window through the first wiring layer and a portion of a second wiring layer in one single step.

Because these inventions are distinct for the reasons given above, the inventions have acquired a separate status in the art because of their recognized divergent subject matter as shown by their different classification, the search required for Group II is not required for Group I, and separate examination would be required, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

During a telephone conversation with Richard J. Botos on December 10, 2001 a provisional election was made with traverse to prosecute the invention of group I (the integrated circuit), claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action. Claims 9-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Roy.

Regarding claim 1, Roy discloses on figure 13 an integrated circuit comprising "a semiconductor substrate including semiconductor devices; a first wiring layer [522] having an associated thickness being located over the substrate and having interconnect wire [520] embedded therein; a second wiring layer [530] having an associated thickness located on the first wiring layer and having interconnect wire [502] embedded therein; and a capacitor having a first metal based charge storage electrode [504], a second metal based charge storage electrode [506], and a dielectric layer [508] interposed between the charge storage electrodes, the charge storage electrodes extending through the thickness of the second wiring layer [530] and at least part of the first wiring layer [522]". Note that it is well known in the art that the substrate is used as a layer on which the other layers of the integrated circuit are formed. Therefore, it is inherent that the structure shown on figure 13 by Roy would have a substrate.

Regarding claim 2, Roy discloses on figure 13 that the dielectric layer 508 comprises one if Ta_2O_5, $BaSrTiO_4$ (col. 11, lines 21-24).

Regarding claim 7, Roy discloses on figure 13 at least one of the wiring layers is a dual damascene wiring layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinkawata in view of Ma et al.

Regarding claims 1, and 2, Shinkawata discloses on figure 1 substantially all the structure set forth in the claimed invention except the charge storage electrodes based on metal. However, Ma et al discloses on figure 1 the charge storage electrodes 30, 26 (col. 5, lines 40-43) are based on metal. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shinkawata by having the charge storage electrodes based on metal for the purpose of obtaining a high capacitor capacity.

Regarding claim 3, Shinkawata discloses on figure 1 a first region of the substrate includes dynamic random access memory cells; a second region of the substrate 1 includes logic circuits and is physically separated from the first region; and

the capacitor is located in portion of the wiring layers located over the first region of the substrate.

Regarding claim 4, Shinkawata discloses on figure 1 the capacitor is a functional portion of one of the random access memory cells.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinkawata as applied to claim1 above, and further in view of Ma et al.

Regarding claim 5, Shinkawata discloses substantially all the structure set forth in the claimed invention except a third wiring layer being located on the second wiring layer and having a metal based interconnect wire. However, Ma et al discloses on figure 1 a third wiring layer 58 being located on the second wiring layer 38 and having metal based interconnect wire 60 embedded therein, the first charge storage electrode 30 of the capacitor being in physical contact with a portion of the interconnect wire 60 of the third layer. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Shinkawata by having a third wiring layer being located on the second wiring layer and having a metal based interconnect wire for the purpose of increasing the effectiveness of the electrical interconnect in an integrated circuit.

Claims 6- 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinkawata as applied to claim1 above, and further in view of Ma et al.

Regarding claims 6- 8, Shinkawata discloses substantially all the structure set forth in the claimed invention except a tungsten plug being located between the second charge storage electrode and a portion of the substrate. However, Ma et al discloses on figure 1 a tungsten plug 24 being located between the second charge storage electrode 26 and a portion of the substrate 20. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Shinkawata by having a tungsten plug being located between the second charge storage electrode and a portion of the substrate for the purpose of improving the electrical connection in a memory cell.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6078072 to Okudaira et al discloses a semiconductor device suppressing current leakage.

US Patent 6265778B1 too Tottori disclose a semiconductor device with a multi interconnection structure.

US Patent 5471418 to Tanigawal discloses a DRAM with improved stacked capacitor memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
December 11, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800